Notice of Allowability	Application No.	Applicant(s)	
	10/020,426	CASTAGNOZZI ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the Amendment - After Non-Final Rejection filed 08/10/2005*.

2. ☒ The allowed claim(s) is/are *17-48*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JOSEPH TORRES
PRIMARY EXAMINER

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

The Examiner has presented many 112 rejections in this case. The Examiner still has reservations about the claim language. However the Affidavit filed 08/10/2005 by the Applicant makes clear the intended meaning of the language in independent claims 17 and 33 and the Examiner sees no point in doing another round of 112 rejections.

In particular, the last paragraph on page 2 of the Affidavit recites, "The basic components of the Applicants claims are a multi-threshold circuit and a non-causal circuit. The multi-threshold circuit provides a 'plurality of bit estimates' **for each input signal**. As seen in Fig' s. 7A and 7B, in one implementation, the bit estimates are a measurement of the input signal that is responsive to three different threshold levels. Andresen describes a composite threshold circuit with a feedback adjustment mechanism. However, Andresen does not describe a circuit that provides **a plurality of bit estimates for each input data**, as recited in Applicant's claims 17, 33, and 35. Andresen provides a single 'estimate' for each input signal" [Emphasis Added]. The Examiner asserts that although the Applicant never uses the term "**a plurality of bit estimates for each input data**" that the Applicant clearly regards the term "**a plurality of bit estimates for each input data**" as a distinguishing feature. It should be clear that the Applicant interprets "a plurality of bit estimates for each data" in claims 33 and 35 as "**a plurality of bit estimates for each input data**". Likewise, it should be clear that the Applicant interprets "a plurality of bit estimates for each NRZ data" in claim 17

as --**a plurality of bit estimates for each NRZ input data**--. The Examiner disagrees with the Applicant's affidavit that "Andresen does not describe a circuit that provides "**a plurality of bit estimates for each input data**" since input data is a relative term and can include more than one input such as the 9 inputs from the different tracks in Andresen in which case the input data comprising the 9 inputs does produce a plurality of bit estimates.

The second paragraph on page 3 of the Affidavit also recites, "Second, **the non-causal circuit is not an analog feedback circuit**. In a sense, **it includes a '*digital* feedback'** component, but even this explanation misses the mark. The circuit compares bit decisions of different clock periods. I am aware of conventional circuitry that integrates voltage signals (using 'past' **analog** information) in the calculation a current clock bit decision. However, I am unaware of any conventional circuits that use past (***digital***) decisions in the calculation of a current clock decision. This factor, by itself, makes the Applicant's claims novel. However, the non-causal circuit goes a step further and uses both past and 'future' **digital** decisions in the calculation of the present bit decision. Again, I find this factor completely unique in the art". The Examiner agrees with this assessment, but would like to make clear that although the Applicant never refers to **'*digital* feedback'**, "past (***digital***) decisions" or 'future' **digital** decisions in claims 17, 33 and 35, it should be clear that the applicant is interpreting "a non-causal circuit having inputs to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing bit estimates for the current clock cycle, to bit values determined in prior and subsequent

clock cycles" in claim 17 as --a non-causal circuit having inputs to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing bit estimates for the current clock cycle, to **digital** bit values determined in prior and subsequent clock cycles--. The Examiner agrees that Andresen does not teach --a non-causal circuit having inputs to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing bit estimates for the current clock cycle, to **digital** bit values determined in prior and subsequent clock cycles-- as suggested by the Applicant's affidavit. It should also be clear that the Applicant is interpreting "a non-causal circuit having an input to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing bit estimates for the current clock cycle, to bit values determined in prior and subsequent clock cycles" in claims 33 and 35 as --a non-causal circuit having an input to accept the bit estimates from the multi-threshold circuit and an output to supply a first bit value for a current clock cycle in response to comparing bit estimates for the current clock cycle, to **digital** bit values determined in prior and subsequent clock cycles--.

The Examiner would also like to point out that the Examiner has given patentable weight to the term "non-causal channel equalization communication system" [Emphasis added] in the preambles of claims 17, 33 and 35 in the Examiner's search since the Applicant only teaches the body of claims 17, 33 and 35 for a "non-causal channel equalization communication system" in the Applicant's specification; hence the body of the claims do not warrant a search of every possible circuit outside of a "non-causal

channel equalization communication system" that may use the arrangements in claims 17, 33 and 35.

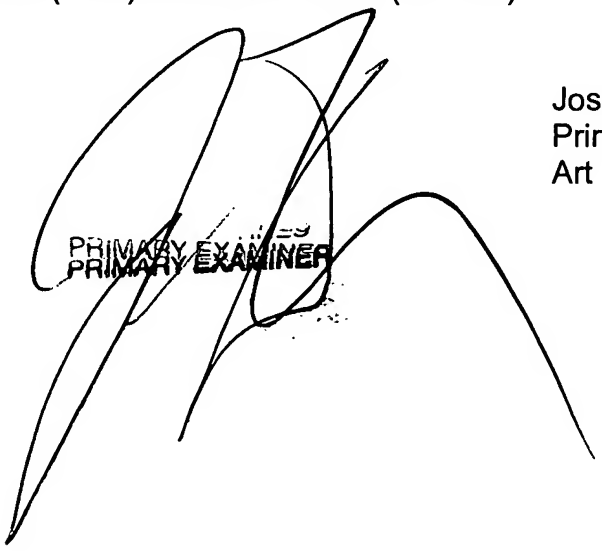
Ordinarily, the Examiner would hold out till the Applicant amended the claims to clarify the Applicant's invention, however, prosecution for this case has gone on for too long, and as pointed out, above, the record is clear on what the Applicant regards as his invention (Note: the Examiner has done 3 non-finals for his case and a final and any further actions on this case would represent an undue burden for the Examiner, in view of the fact that the record makes clear the Applicant's invention as well as the limitations in the Examiner's search, see the Non-Final Rejection filed 07/13/2005), although, in the Examiner's opinion the claim language of claims 17, 33 and 35 still suffer from deficiencies, as pointed out above, in pointing out what the Applicant regards as his invention.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (571) 272-3829. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Joseph D. Torres, PhD
Primary Examiner
Art Unit 2133